REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-14 are pending in this case. Claim 1 is amended herein and claims 10-14 are added herein.

The Examiner rejected claims 1-9 under 35 U.S.C. §103(a) as being unpatentable over Jang et al. (U.S.6,019,906) in view of Grill et al. (US 6,140,226).

Applicant respectfully submits that claim 1 is patentable over the references as there is no disclosure or suggestion in the references of extending a via, depositing a BARC layer within the via such that the BARC layer is significantly thicker in said via than over the hardmask, forming a trench pattern over the BARC layer, and etching a trench. Jang et al teach patterning and etching a hardmask and dielectric layer. As the Examiner pointed out, Jang does not teach depositing a BARC layer over the hardmask and within a via, forming a trench pattern over the BARC layer or etching a trench in the intrametal dielectric. Grill teaches a dual damascene process that includes the step of depositing a thin conformal liner over a hardmask and within a via. However, the teaching of a thin conformal liner does not disclose or suggest to one of ordinary skill in the art depositing a BARC layer within the via such that the BARC layer is significantly thicker in the via than over the hardmask. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are patentable over Jang in view of Grill.

Applicant respectfully submits that newly added claim 10 is patentable over th references as there is no disclosure or suggestion in the references of extending the via by selectively etching the intrametal dielectric layer and the

shelf layer and depositing a BARC layer over the hardmask and within the via after the extending the via step. Grill only teaches etching the top (intrametal) dielectric before forming the thin conformal liner.

Applicant respectfully submits that newly added claim 11 and the claims dependent thereon are patentable over the references as there is no disclosure or suggestion in the references of extending the via by selectively etching the intrametal dielectric layer and the interlevel dielectric layer and then depositing a BARC layer over the hardmask and within the via. Grill only teaches etching the top (Intrametal) dielectric before forming the thin conformal liner.

Attached hereto is a marked up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with Markings to Show Changes Made.**"

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-14. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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Version with Markings to Show Changes Mad

Claim 1 is amended as follows:

1. (amended) A method of fabricating an integrated circuit, comprising the steps of:

forming an interlevel dielectric layer over a semiconductor body;

forming an intrametal dielectric layer over said interlevel dielectric layer;

forming a hardmask over said intrametal dielectric layer;

forming a via pattern over said hardmask;

selectively etching a via through said hardmask;

extending said via by selectively etching said intrametal dielectric layer;

depositing a BARC layer over said hardmask and within said via, wherein said BARC layer is significantly thicker within said via than over said hardmask;

forming a trench pattern over said BARC layer; and

etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via.

Claims 10-14 are added.